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INDIA-TAIWAN COLLABORATION IN THE GEOPOLITICS OF A DEFENCE FOUNDRY POWER

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INDIA-TAIWAN COLLABORATION IN THE GEOPOLITICS OF A DEFENCE FOUNDRY POWER



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Abstract

At the global semiconductor order today, Taiwan sits at the centre when it comes to frontier fabrication and back-end processes involving assembly, testing, and advanced packaging. The most significant part is that this centre stage it holds is created by the three linked science-park clusters in a period of five decades. The article makes an effort to understand this aspect and how India can extract from this model to strengthen its ecosystem for its own defence industrial needs. Nonetheless, the restrictions imposed by the Wassner Arrangement and international Traffic in Arms Regulations (ITAR) remain a concern along with TSMC's absence or active engagement with India. The article further discusses the challenges faced by the two countries to facilitate a smooth collaboration in this sector, along with a few mitigation policies.

Introduction

As known as the new oil of the twenty-first century, semiconductors have completed a total transformation and become the substrate of national power. This power can be termed as foundry power. Countries who control this foundry power will make the most advanced chips and will lead in military strength too. Today Taiwan is leading when it comes to the most advanced nodes, including 3nm and 2nm chips. In fact, this foundry power is not just an industrial capacity but a leverage to lead in the geopolitics of the globe.

India, on the other hand, is strengthening its semiconductor ecosystem through initiatives such as India Semiconductor Mission (ISM) 1.0 and the ISM 2.0. This is leveraged through its vision of Amrit Kaal and to achieve Atmanirbharta in this sector. Today, semiconductors are not merely an emerging technology but a capability that enhances the nation's position and control in the globe, considering the fact that they form the backbone of advanced military technologies.

At this point, the article examines three tiers of cooperation with Taiwan: capital and investment cooperation, cooperation in packaging and defence industrial collaboration. While seeing the India-Taiwan relationship from this lens, India today sits in the first tier while making a partial move towards the second, followed by efforts to scale up its presence in the third tier.

Taipei's Lead in Foundry Power

Taiwan's position at the apex of the global semiconductor order is the product of a deliberate, five-decade state project rather than an accident of geography. The starting point is 1973, when Taiwan established the Industrial Technology Research Institute (ITRI) to anchor the island's investment in semiconductor research and development.¹ Three years later, in 1976, ITRI signed a technology-transfer and licensing agreement with the American firm Radio Corporation of America (RCA), which allowed Taiwan to import the know-how to build 3-inch wafers.² That transfer of knowledge produced Taiwan's first integrated circuit production line and laid the foundation for what would

become a vertically specialised supply chain, in which numerous independent Taiwanese firms each handle a distinct stage of production rather than one company attempting to own the whole process.³ By 1987, this foundation had matured into Taiwan Semiconductor Manufacturing Company (TSMC), which would become the world's most advanced semiconductor foundry.⁴ Between 2000 and 2010, Taiwan consolidated its position as the global leader in semiconductor manufacturing, and in August 2022, it formalised this dominance further with the launch of the Southern Taiwan Semiconductor Corridor across the Kaohsiung and Tainan regions.⁵

Two Structural Factors Behind Taiwan's Rise

Beyond the institutional timeline, it is worth discussing what actually made this possible, since these are the factors, India is now trying to replicate to an extent. The first was a shift in technology and business models beginning in the 1980s. As capital expenditure requirements for semiconductor manufacturing rose sharply, TSMC recognised an opportunity to pioneer the "pure-play" foundry model, producing bespoke chips solely for other companies' designs, whether fabless chip-design firms or, more recently, integrated device manufacturers such as Intel, rather than designing and selling its own branded chips.⁶ The second was the availability of a deep pool of skilled engineering talent, much of it trained abroad and repatriated to Taiwan at precisely the moment the industry needed it.⁷ Neither factor was inevitable; both were the product of policy choices sustained over decades, and both bear directly on what India can plausibly replicate on a shorter timeline.

Current Standing

The payoff of this trajectory is stark. TSMC alone produces more than 90 per cent of the world's most advanced chips and occupied over 70 per cent of the global foundry market in 2025.⁸ Since its commercial launch in 2022, TSMC's 3 nm process has become the industry standard for high-performance computing, artificial intelligence, and mobile devices, while its 1.6 nm process is scheduled to enter commercial production in the second half of 2026, evidence that TSMC's edge rests on a sustained cadence of innovation rather than a single technological leap.⁹ Notably, even TSMC's overseas expansion has stayed almost entirely at the leading edge. All three of its investments in the United States since 2020, totalling approximately USD 65 billion,

have gone into advanced fabrication; its co-investment in Germany is a "speciality technology fab"; and its majority-owned Japanese subsidiary, Japan Advanced Semiconductor Manufacturing (JASM), is building 6nm and 7nm capacity for automotive, industrial, and high-performance computing applications. This is done while continuing mature-node production down to 40nm.¹⁰ The common thread is unmistakable: wherever TSMC itself invests abroad, it invests in fabrication and overwhelmingly at the advanced or speciality end.

The Front-End/Back-End Distinction

When there is a concern with what India can realistically extract from Taiwan's model, one distinction matters more than any other, i.e., the difference between front-end fabrication and back-end involving assembly, testing, and packaging (ATP). Before a chip can power an AI server, a smartphone, or a missile-guidance computer, it must pass through a series of highly specialised back-end processes that transform a fabricated wafer into a reliable, deployable product.¹¹ Assembly slices a large, newly fabricated wafer into distinct miniature squares, testing simulates years of real-world stress to filter out anything failing strict performance metrics, and packaging completes the process by preparing verified chips for integration and distribution.¹² As chips grow more complex, these downstream capabilities have become just as critical as fabrication itself, and, crucially, this is also the segment of the value chain where India's entry is realistically achievable. In 2023, Taiwan's packaging and testing sector alone captured more than 50 per cent of the global market, generating NTD 584 billion (roughly USD 18.46 billion) in revenue.¹³ Five of the world's ten largest semiconductor assembly and testing companies are headquartered in Taiwan, led by ASE Group, the world's largest independent provider of chip assembly and testing services.¹⁴ Most commentary on Taiwan focuses almost entirely on TSMC and its cutting-edge chips, overlooking the massive back-end industry behind it. But that's exactly the part India should be paying attention to, since it is not competing with TSMC at the leading edge in the immediate term.

The Second Foundry Power: CoWoS and Advanced Packaging

Within this back-end universe, one technology deserves particular emphasis. It is Chip-on-Wafer-on-Substrate (CoWoS) packaging, TSMC's method of bonding logic

dies and high-bandwidth memory onto a wafer before mounting the assembly onto a substrate so that multiple chips function as an integrated whole. This is the process underpinning today's AI accelerators and GPUs. Packaging innovation is fast becoming as strategically consequential as node width itself. For defence applications specifically, ruggedised radar modules, electronic-warfare payloads, and secure-communications hardware that must integrate multiple heterogeneous components into a single hardened unit, advanced packaging capability may matter more than raw access to a 2-nm node. This reframes what "catching up with Taiwan" should mean for India. It is not a race toward the leading node, which is neither necessary nor attainable in the medium term, but a race toward packaging sovereignty.

The Upstream Materials

Beneath both fabrication and packaging sits a further dependency layer. They are the raw and processed materials, silicon wafers, photoresists, photomasks, and speciality gases, without which no fabrication or packaging facility can operate. Taiwan, alongside South Korea and China, sits among the handful of economies dominating this layer. It receives far less attention than fabrication headlines, yet it represents an equally serious chokepoint for any state, India included, attempting to build defence-electronics supply security. Sovereign packaging or fabrication capacity is of limited strategic value if the underlying materials must still be imported from a small number of foreign suppliers.

Taiwan's Cluster Architecture

Taiwan's cluster model is not confined to Hsinchu alone. It has matured into three linked hubs running the length of the island's western corridor, each with a distinct role.

- Hsinchu Science Park (north), the original, established in 1980. This is Taiwan's Silicon Valley equivalent, with about 900 semiconductor companies and roughly 170,000 workers packed into just 15 square kilometres, including TSMC and MediaTek, right next to National Yang Ming Chiao Tung University and ITRI. The density is the point: engineers move between firms by scooter, and the whole park's annual revenue is expected to top USD 56.9 billion in 2026.¹⁵

- Southern Taiwan Science Park (Tainan/Kaohsiung), the "Southern Silicon Valley." This is the closest equivalent to Japan's Kyushu corridor. It groundbreaks in 1996 and now oversees six sub-parks, Tainan, Kaohsiung (Luzhu), Ciaotou, Nanzih, Chiayi, and Pingtung, across more than 2,900 hectares. TSMC's 2022 groundbreaking for new fabs sits inside this corridor, at Nanzih. In early 2025, the government formally approved a "Southern Silicon Valley" initiative to knit these sites together, and by mid-2025, this southern cluster alone was generating over NT\$1.38 trillion in half-year revenue, more than half of all three parks' combined output.
- Central Taiwan Science Park (Taichung), the newer, third pole. Founded in 2003, historically smaller, but now being built up specifically as Taiwan's next-generation fabrication hub (reportedly aiming at 1.4 nm-class capacity by 2028), designed explicitly to link Hsinchu and the south into one continuous "western corridor technology spine". There's also a newer, more specialised addition worth flagging, specifically how Taiwan just broke ground on its first dedicated "special semiconductor supply chain park" in Pingtung County (mid-2026). It aimed at resilience, bringing in advanced facility engineering and cleanroom construction firms rather than chipmakers themselves, to shore up the supply chain feeding the other clusters.¹⁶

What Taiwan's Cluster Model means for India

The lesson here is not simply that clustering helps; India's own semiconductor parks in Gujarat already gesture at this, but that Taiwan's three hubs function as a linked system rather than three competitors for the same investment. Hsinchu supplies the design and research base, the south absorbs the largest new fabrication capacity, and the centre is now being built specifically to connect the two into a single western-corridor spine.¹⁷ India's current semiconductor geography, by contrast, is closer to where Taiwan stood before this linkage was deliberate: Dholera, Jewar, and Sanand each operate as standalone sites, competing individually for Taiwanese and other foreign investment rather than reinforcing one another.¹⁸ For India to match Taiwan's compounding effect, its parks in Gujarat, Tamil Nadu and Assam need corridor links,

not just co-location. Gujarat brings ports, industrial inputs and a strong fab policy push. Tamil Nadu brings the chip demand, with its electronics, phone and auto clusters. Assam adds low-cost assembly and an eastward gateway to Southeast Asia, so together they form one value chain.

A Closer Parallel than Japan's Kyushu Model

Taiwan's supply chain integration effort with Japan's Kyushu region is worth noting while discussing clusters. That arrangement is a bilateral link, feeding component suppliers into a foreign partner's fabs. Taiwan's own domestic clustering is a more ambitious and more relevant template for India specifically, since it shows how a state can consciously sequence its own science parks, an original hub for research and design, a second for volume fabrication, and a third purpose-built to connect the two, rather than leaving each site to develop in isolation. India's Semiconductor Mission could reasonably borrow this sequencing directly. This could be done by treating Gujarat's existing momentum as its "Hsinchu", using Tamil Nadu or Assam's newer parks as deliberate extensions rather than parallel bets, and designing the connective infrastructure between them as a named policy objective in its own right, the way Taiwan's Executive Yuan formally approved its "Southern Silicon Valley" initiative to do exactly this in January 2025.

Why India, specifically, and not simply "any Taiwan partner"?

India is not trying to compete in advanced fabrication yet. It has instead deliberately gone after mature-node production above 40nm, where the near-term growth potential looks more realistic. This calibrated positioning is visible in the 2022 adjustment to India's semiconductor subsidy framework, which now offers equal subsidies to mature and advanced nodes alike.

The Tata-PSMC venture bears this out. Available evidence suggests PSMC likely opted for technology transfer rather than committing large amounts of capital. The plant itself is understood to target mature-node technologies in the 28 nm, 40 nm, 55 nm, 90 nm, and 110 nm ranges. It has reportedly already secured orders from Tesla for its worldwide operations.

It is worth comparing this to Malaysia, which is often seen as better positioned. Malaysia has an OSAT ecosystem dating back to Intel's 1972 Penang facility, and it is part of the Regional Comprehensive Economic Partnership (RCEP). However, New Delhi's position is considered to be more favourable here, since Malaysia has been more dependent on Chinese manufacturers when it came to the OSAT relocation. This is again followed by cybersecurity-related risks and export control. Moreover, Malaysia has not made a shift from the OAST hub to the value chain of chip design. In this context, India seems to be a little different, especially when it comes to design. It has roughly a quarter of the global design workforce for chips.¹⁹ That workforce is increasingly trained in "digital twinning", the virtual representation of a semiconductor fabrication environment. Firms like Lam Research have already set up a "virtual nano-fabrication environment" in India to support exactly this kind of work. This is a genuine comparative advantage.²⁰

The "Silicon Shield" and its Formal Architecture.

Taiwan's chip dominance has long worked as an informal deterrent, a "silicon shield", whose value to the world discourages anyone from disrupting it. What has changed is that this idea now has real institutional form.

In December 2025, the US launched Pax Silica, an initiative to build secure, allied supply chains for the technologies underpinning the AI era, semiconductors, critical minerals, manufacturing, compute, and energy. India was not part of the initial group that signed on in Washington that month. It joined later, on 20 February 2026, signing the Pax Silica Declaration at the India AI Impact Summit in New Delhi, alongside broader talks on defence cooperation with Washington.²¹ Taiwan's position here is more complicated. As of mid-2026, it is still not a full signatory, just a participant. That is mostly down to the diplomatic sensitivities around the One China Policy, even though Taipei has backed the declaration's principles.²²

This distinction is that India now sits inside a US-led framework built specifically to protect the chip supply chains Taiwan dominates, while Taiwan itself remains just outside that formal structure. So, India's cooperation with Taiwan on semiconductors runs alongside this multilateral framework, not through it. And that is exactly why a

defence dimension of India-Taiwan cooperation is likely to stay implicit rather than explicit.²³

Silicon Dominance to R&D for Compound Semiconductors

Taiwan's semiconductor ecosystem, built on foundry excellence and advanced packaging, plays a genuinely important enabling role in fabricating GaN and SiC devices for both domestic and global customers.²⁴ Crucially, however, this strength sits disproportionately on the fabrication and packaging side of the compound-semiconductor chain rather than in upstream substrate and material growth, where Japanese firms (Rohm, Mitsubishi Electric, Fuji Electric and Toshiba) and Chinese vertically integrated players (Innoscence on GaN-on-Si and BYD Semiconductor on SiC MOSFETs) currently hold stronger positions.²⁵ Notably, TSMC itself has largely stayed out of the SiC substrate market while choosing instead to let device fabrication and packaging. That remains its point of entry rather than raw material production. Hence, Taiwan's compound-semiconductor advantage is best understood as an extension of its packaging and heterogeneous-integration strength but not as dominance across the entire material stack.²⁶

However, Taiwan's National Science and Technology Council (NSTC) has stated explicitly that Taiwan will continue advancing R&D in compound-semiconductor devices, modules, and systems. They have already pushed for strengthening the domestic capability in GaN-on-X platforms and 8-inch, potentially 12-inch, SiC substrate technologies. This is seen as an active positioning already underway in Ga₂O₃ alongside heterogeneous integration.²⁷ To this end, the NSTC is launching an Advanced Research Program on High-Performance Compound Semiconductors in 2026, aimed at meeting shared requirements across EVs, smart grids, and renewable-energy power conversion, with the explicit goal of developing high-reliability wide-bandgap semiconductor and module technologies.²⁸ Taiwan had already set a target of achieving self-supply of 8-inch SiC wafers and associated equipment in 2025. Its broader chipmaking supply chain has been actively working to forge a domestic GaN ecosystem around this same window.²⁹ Industry activity backs this up. Actron, an automotive power-device maker, has been scaling up its SiC output. Hua Hsu Silicon Materials is expanding its SiC wafer production. And a more diversified player, Tai Asia Semiconductor, is even absorbing near-term losses just to get new SiC and GaN

business lines off the ground.³⁰ SEMICON Taiwan 2026, the largest semiconductor industry event, spanning 1,200 exhibitors and over 20 international forums, listed compound semiconductors and heterogeneous integration among its eight headline industry themes for the year, a reasonable proxy for how central this segment has become to Taiwan's forward strategy.³¹

A 2026 memorandum of understanding (MoU) between Taiwan-based GeChi Compound Semiconductor (GCCS) and Purdue University, United States focuses jointly on isolating crystal defects and optimising SiC material growth. This is to accelerate the transition to high-yield 8-inch and 12-inch wafer platforms, explicitly targeting the thermal, power, and 6G bottlenecks constraining next-generation high-compute infrastructure.³² Such initiatives reflect university-industry-government linkage while mirroring the ITRI-academia model as discussed earlier. India's own compound-semiconductor ambitions could replicate this template. DRDO's laboratories and Indian technical universities could plausibly seek to join it, or mirror it through a parallel arrangement, rather than starting from a blank page.

All of this matters enormously, but it should not obscure a harder structural fact that even a fully willing Taiwanese partner cannot legally close India's defence-semiconductor gap on its own. Regimes such as the Wassenaar Arrangement and the United States International Traffic in Arms Regulations (ITAR), alongside the dual-use Export Administration Regulations (EAR), which more often govern advanced chip and packaging technology, constrain how much frontier semiconductor IP can legally move to India for military end-use. This is regardless of Taipei's intentions or India's diplomatic standing with Taiwan. These frameworks exist independently of any bilateral goodwill between New Delhi and Taipei, since they are administered by Washington and apply to any third-country transfer involving US-origin technology or design tools embedded somewhere in the supply chain, and given how deeply American IP runs through Taiwan's own semiconductor ecosystem, Taipei often has limited room to manoeuvre even when it wants to help. As a result, the ceiling on cooperation is not a matter of trust or intent between the two countries but a legal architecture neither side fully controls.³³

Structural Challenges

There exist a few areas where India and Taiwan find it a little challenging to strengthen their collaboration in this sector. Some of them have been discussed in the following paragraphs:

- **Absence of the Frontier Player.** TSMC itself has not been able to show a significant level of interest in greenfield fabrication investment in India. Rather, it chose to concentrate its overseas bets on the US, Japan, and Germany. India's Taiwan relationship, at the frontier level, currently runs through PSMC. It is a capable but second-tier foundry rather than the world's leading node. This limits how far "cooperation with Taiwan" can substitute for genuine access to cutting-edge fabrication.
- **Political Sensitivity Ceiling.** India's calibrated China policy shapes how openly it can engage with Taiwan. New Delhi's continued hesitation on a Taiwan free trade agreement, despite Taipei's own eagerness, reflects this caution directly. Any defence dimension of India-Taiwan cooperation is therefore likely to stay implicit and dual-use rather than openly declared as military cooperation.
- **Export-control Architecture.** Regimes such as the Wassenaar Arrangement and the United States ITAR constrain how much frontier semiconductor IP can legally move to India for military end-use. This ceiling applies regardless of Taipei's willingness to cooperate, since much of Taiwan's own technology stack is itself entangled with US-origin IP and design tools.
- **Infrastructure and Talent Gaps.** Semiconductor manufacturing remains a capital- and infrastructure-intensive undertaking, and India continues to face real gaps in power reliability, water availability, and investment scale. India has a large pool of skilled labour overall, but engineers with specific expertise in process technology and device physics remain in short supply.
- **Supply-chain integration lag.** Taiwan's ongoing supply-chain integration effort with Japan, anchored around a dedicated industrial park in Kyushu feeding TSMC's Japanese operations, shows how Taiwan prefers to invest where an enabling ecosystem already exists. India's own supply chain integration remains comparatively nascent by this benchmark, and closing that

gap is a precondition for attracting deeper Taiwanese investment, defence-relevant or otherwise.

Strategic Recommendations

To mitigate the challenges faced by the two nations to initiate a proper collaboration in this sector, there are a few aspects which could be addressed at the government, academic, and industry levels. Some of them have been highlighted in the following paragraphs:

- **Establish an India-Taiwan Semiconductor Desk within MEITY.** This directly addresses the political sensitivity ceiling. A dedicated desk, expanded to include a liaison function with DRDO and India's defence-indigenisation apparatus, can operate through existing quasi-diplomatic channels rather than a formal state-to-state defence pact, working within India's One China Policy constraints rather than against them.³⁴
- **Leverage PLI-DLI Incentives with a Defence-Electronics Qualification Track.** This responds to the infrastructure and talent gap. Using India's Production Linked Incentive and Design Linked Incentive schemes deliberately, with a specific sub-track calibrated to defence-electronics qualification standards, could help attract Taiwanese firms and design-ecosystem players even without TSMC's direct participation.³⁵
- **Pursue a Co-development Model through Joint Semiconductor Parks.** This is the direct answer to the supply-chain integration lag. Inviting Taipei to help establish joint semiconductor parks in Gujarat, Tamil Nadu, and Assam, structured with dual-use zoning, would replicate the clustering logic behind Taiwan's own Kyushu integration effort with Japan rather than leaving India to build this ecosystem in isolation.
- **Deepen R&D collaboration with ITRI, TSMC, UMC, and Taiwanese academia.** This offsets both the talent gap and TSMC's absence from Indian fabrication. Formal research partnerships, directed specifically toward compound-semiconductor and RF/microwave device research, allow India to draw on Taiwan's frontier expertise even where direct fabrication investment is not forthcoming.

- **Build CoWoS-type Packaging Capability Oriented Specifically to Defence Electronics.** Since India is not seeking immediate access to the leading fabrication node, advanced packaging, and heterogeneous integration for radar and EW payloads, it offers a realistic substitute source of strategic value. In fact, this is very much achievable without waiting on frontier node access.
- **Shift Policy from a Commercial-Chip Strategy to an Explicitly Defence-Centric Semiconductor Strategy.** This is the direct response to the export-control architecture. Since Wassenaar and ITAR restrictions mean frontier IP cannot simply be imported even under a willing partnership. India's semiconductor policy, built so far around PLI, DLI, and ISM, needs a defence-centric layer with its own funding lines and qualification standards, layered on top of the commercial base rather than substituting for it.
- **Use Multilateral Cover Including Pax Silica and the QUAD's Critical and Emerging Technology Vertical, to Deepen Ties while Managing China Sensitivity.** This reinforces the response to the political sensitivity ceiling. Multilateral frameworks give India a way to advance Taiwan-linked semiconductor cooperation without forcing an explicit bilateral defence declaration, reducing the diplomatic exposure a purely bilateral arrangement with Taipei would carry.

Conclusion

There exists a significant level of potential between India and Taiwan to collaborate in strengthening the semiconductor ecosystem, mostly to cater to the needs of the Indian military systems. Although Taiwan is a powerhouse of foundries, its lead in back-end processes is something which India can extract. Hence, it could be highlighted that not fabrication sovereignty, but packaging sovereignty, is achievable. Taiwan's cluster model reinforces this. Hsinchu, the south, and the centre were never meant to compete with each other; rather, they were built to extend one another. India's parks in Gujarat, Tamil Nadu, and Assam could consider the same logic: not standalone bets, but a deliberate corridor, each site strengthening the next.

Yet none of this cooperation can be treated as sufficient on its own. Export-control regimes sit above Taipei's intentions and India's ambitions alike, placing a hard ceiling on what technology can legally move between the two, regardless of goodwill.

However, to conclude, Taiwan's role, in the end, extends beyond commerce; it helps build the platform on which India's defence capability can also stand, not just its commercial one. What gets built on top of that platform, in defence-grade packaging and compound-semiconductor R&D, is India's alone to shape, and that work needs to start now.

Declaration

I declare that this manuscript is being submitted exclusively to CENJOWS for publication consideration, is original, and has not been published or submitted elsewhere. I further certify that it contains no classified, restricted, or sensitive information and is based entirely on open-source material suitable for publication in the public domain.

ENDNOTES

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