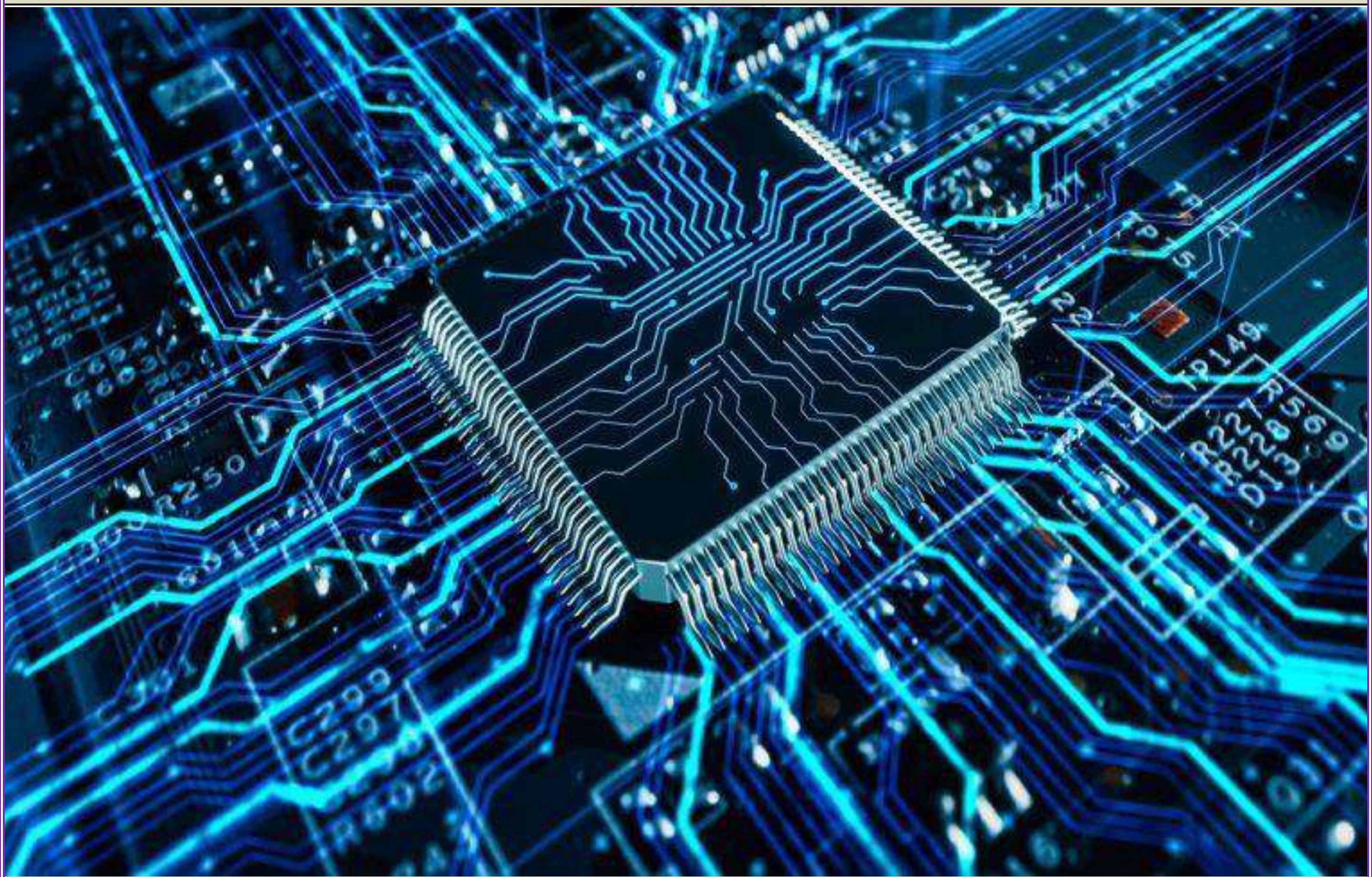
POLICY RECOMMENDATIONS REPORT

ON

"2nd WORKSHOP ON ENERGIZING SEMICONDUCTOR ECOSYSTEM FOR DEFENCE APPLICATIONS"



WORKSHOP CUM EXHIBITION

"2nd WORKSHOP ON ENERGIZING SEMICONDUCTOR ECOSYSTEM FOR DEFENCE APPLICATIONS"

(ORGANISED BY SA TO CISC IN COLLABORATION WITH CENJOWS)

ON 07 APR 26

1. Semiconductors form the technological backbone of modern defence systems, enabling capabilities across radar, electronic warfare, satellites, cyber systems, AI-enabled warfare, and secure communications. Their dual-use nature makes them central to both economic competitiveness and national security. Globally, semiconductor production is highly concentrated (e.g., US, Taiwan, South Korea), creating strategic vulnerabilities for countries dependent on imports. India, despite having a strong design talent base, remains heavily reliant on foreign semiconductor supply chains. To bolster indigenous efforts in design, fabrication, packaging, and testing of Semiconductors, the India Semiconductor Mission (ISM) has engendered a robust ecosystem driven by academia and industry. For defence, semiconductor capability is not just an industrial goal—it is a strategic imperative for sovereignty, resilience, and technological superiority.

2. India Semiconductor Mission (ISM) 1.0 was launched in Dec 2021 with the objective of reducing reliance on chip imports and creating a self-reliant electronics manufacturing ecosystem. With the progress of time, defence forces decided to become an active stakeholder. HQ IDS (Office of SA to CISC), organised the first workshop on "Energising Semiconductor Ecosystem to Make India Self-Reliant in IC Chip Manufacturing" on 13 Dec 2024, the deliberations of which were shared with stakeholders in the form of a Policy Recommendation Report. The initiative of the first workshop on 13 Dec 2024 was carried forward by conducting the second workshop cum exhibition on 07 Apr 2026, wherein participation of all stakeholders was ensured.

3. ISM 2.0 was launched during the Union Budget 26–27, which marks a strategic shift from initial ecosystem creation to deep capability building and global integration. The conduct of **Operation Sindoor** also established an undisputed need for military applications to be based on indigenous chips.

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4. The event was aimed to bring together the representatives of defence services, paramilitary forces, DRDO, PSUs, academia and industry with an objective to amalgamate the specific requirements, expertise and capabilities to handle the associated challenges. The event witnessed more than 250 attendees of various categories and 23 industries exhibiting their products. The keynote address by Air

Marshal Praveen Keshav Vohra, UYSM, AVSM, VM, DCIDS (PP&FD) established the tone and tenor of the discussion. In broad terms, the aims and objectives of the event were: -

4.1. To bring together defence forces, DRDO, academia, industry, startups, and policymakers to foster coordinated national efforts for semiconductor development and deployment.

4.2. To promote Whole-of-Nation collaboration by shared infrastructure, joint R&D, and policy alignment to build a resilient and self-reliant national semiconductor ecosystem.

4.3. To assess the current status of India’s semiconductor ecosystem, especially in the context of Military applications.

4.4. To identify Defence-specific Semiconductor requirements and to align operational military needs with semiconductor technology development, including processors, RF components, sensors, secure communications, and AI-enabled systems.

4.5. To enhance Supply Chain Resilience by strengthening domestic capabilities and strategic partnerships to ensure continuity of supply during geopolitical, economic or technological disruptions.

4.6. To promote design-led innovation, domestic IP ownership, and indigenous fabrication capabilities across the semiconductor value chain.

4.7. To enable stronger integration between armed forces, DRDO labs, industry, and academia for faster development and deployment of defence semiconductor technologies.

4.8. To leverage India's Talent and R&D Ecosystem for defence-focused innovation and technology development.

4.9. To explore strategic partnerships with friendly nations for technology sharing, joint development and resilient supply chains while maintaining strategic autonomy.

4.10. To identify emerging semiconductor technologies such as AI chips, quantum devices, photonics, and advanced sensors relevant for future warfare capabilities.

4.11. To identify pain points hindering growth and collaboration efforts and bridge the gap between users, academia, innovators and industry.

4.12. To recommend policy reforms, procurement frameworks, and institutional mechanisms needed to accelerate semiconductor self-reliance for defence applications.

IMPORTANT ASPECTS EMERGED FROM THE WORKSHOP CUM EXHIBITION

5. **Strategic Context**. Semiconductors are now strategic assets which underpin critical defence systems. They are the "strategic high ground" in modern warfare and geopolitics. Important aspects are as under:-

5.1. **Semiconductors as the Centre of Gravity in Modern Warfare.** Semiconductors have become foundation to modern defence systems, including missiles, radars, AI-enabled decision systems, electronic warfare, and secure communications, making technological sovereignty a national security imperative.

5.2. **Rising Geopolitical and Supply Chain Vulnerabilities.** Global semiconductor supply chains are concentrated in a few countries, exposing India to risks of technology denial, export controls and disruptions during geopolitical conflicts.

5.3. **Shift from Platform-Centric to Information-Centric Warfare.** Military operations increasingly depend on data processing, AI, sensing and communication technologies powered by semiconductors, thus compressing the OODA loop and enhancing operational advantage.

5.4. **Defence Self-Reliance as Strategic Necessity.** Over 70% of defence semiconductor components are imported, creating operational vulnerabilities and necessitating the development of indigenous capabilities.

5.5. **Emerging Technologies Driving Semiconductor Demand.** AI, quantum computing, photonics, hypersonic sensors, neuromorphic computing, and advanced communications are driving future semiconductor requirements.

5.6. **Opportunity to Leverage India's Design Talent.** India holds a strong position in global chip design talent, creating an opportunity to pursue design-led semiconductor leadership.

5.7. **Whole-of-Nation Collaborative Approach.** The traditional divide between DPSUs and private industry is diminishing, and a collaborative national innovation model emerges that involves government, industry, academia, and startups.

5.8. **National Policy Push through ISM 2.0.** The Indian Semiconductor Mission (ISM 2.0), with an increase to ₹ 40,000 crores towards the Electronics Components Manufacturing Scheme (ECMS) in Budget 2026-27, reflects a strong government commitment towards building an indigenous semiconductor ecosystem spanning materials, design, fabrication and manufacturing.

5.9. **Defence Forces as Active Ecosystem Partners.** Defence forces are transitioning from end-users to co-developers and demand drivers, actively shaping semiconductor requirements and supporting innovation.

5.10. **Toward Knowledge-Efficient Innovation System.** There is a growing need to accelerate innovation through knowledge sharing, the reuse of IP, and the reduction of duplication of R&D efforts.

5.11. **Toward Self-Reliant and Export-Oriented Ecosystem.** A robust, indigenous semiconductor ecosystem with long-term export potential and global competitiveness is the need of the hour.

6. **Challenges Identified**.

6.1. **Heavy Dependence on Foreign Semiconductor Supply.** India's defence systems rely significantly on imported chips, creating risks related to supply chain disruptions and compromised security.

6.2. **Limited Indigenous Manufacturing Capability.** Domestic fabrication facilities are limited, particularly for advanced nodes, restricting indigenous production capacity.

6.3. **Supply Chain Security and Hardware Integrity Risks.** Offshore fabrication raises concerns of hardware backdoors, trojans, and compromised system integrity.

6.4. **Fragmented Ecosystem and Lack of Coordination.** Multiple stakeholders exist, but coordination among defence forces, DRDO, industry, and academia remains limited.

6.5. **High Capital Investment Requirements.** Semiconductor manufacturing requires significant financial investment and long gestation periods.

6.6. **Talent and Skilled Manpower Gap.** Shortage of trained semiconductor engineers and domain specialists remains a major bottleneck.

6.7. **Limited Domestic IP Ownership.** India's semiconductor patents and IP ownership remain limited compared to global leaders.

6.8. **Obsolescence and Technology Gaps.** Rapid technological advancements create risk of obsolescence in existing indigenous capabilities.

6.9. **Strategic Dependence on Foreign Supply Chains.** The Heavy reliance on imported semiconductors and OEM ecosystems increase exposure to Geopolitical disruptions and Export controls and sanctions.

6.10. **Risk of Supply Chain Weaponisation.** The export controls, technology denial, or supply restrictions by dominant countries to exert geopolitical or economic pressure engender Supply chain weaponisation. Such actions can disrupt access to critical chips, undermining national security, defence readiness, and technological autonomy.

6.11. **Hardware Security & Trust Deficit.** There is a technological limitation to verify the integrity of imported chips, which may contain vulnerabilities, including Hardware backdoors and Malicious design elements. The absence of a robust, trusted semiconductor certification framework is a challenge.

6.12. **Underdeveloped Domestic Manufacturing Capability.** Lack of advanced fabrication (fab) infrastructure and limitations in Packaging and testing. Semiconductor-grade materials need to be addressed to reduce overdependence on global manufacturing hubs

6.13. **Gaps in Defence-Specific Semiconductor Capability.** Military applications require High reliability, extreme-environment tolerance, and long-lifecycle support. The current ecosystem is not fully aligned with defence-grade requirements.

6.14. **Materials & Rare Earth Supply Constraints.** Dependence on imports for critical minerals and semiconductor materials is a major challenge. The recycling ecosystem is still nascent (despite 20–25% potential).

6.15. **Limited Access to Capital & Long Gestation Cycles.** The semiconductor sector is Capital-intensive and high-risk with long ROI timelines. Limited capital availability and targeted funding mechanisms are also a challenge.

6.16. **Absence of Trusted Standards & Certification Systems.** Lack of military-grade semiconductor standards, Insufficient testing and validation infrastructure, Absence of unified framework for quality assurance are also important challenges.

6.17. **Procurement & Demand Uncertainty.** Defence procurement processes are complex and time-consuming. There is also the challenge of lack of demand visibility and long-term procurement commitments which discourages private sector investment.

6.18. **Limited Global Integration with Trusted Partners.** There is a need for deeper collaboration with Trusted technology partners (e.g. Japan, allies). Current partnerships are not fully leveraged for Technology transfer and Joint development.

6.19. **Innovation & Startup Ecosystem Constraints.** Semiconductor startups face high entry barriers, limited access to infrastructure and funding challenges.

6.20. **Gap Between Policy Vision and Ground Reality.** The gap between strong policy intent (vide ISM2.0) and ground readiness levels needs to be reduced.

7. **Pain Points**.

7.1. **Lack of a Clear Defence Semiconductor Roadmap**. Absence of consolidated tri-services demand and long-term planning limits targeted semiconductor development.

7.2. **Slow Development and Procurement Cycles.** Traditional defence development timelines are slow compared to rapidly evolving technology and warfare needs.

7.3. **Limited Industry Participation in Defence Semiconductor Development.** Private industry involvement in defence semiconductor development remains limited and fragmented.

7.4. **Weak Academia–Industry–Defence Linkages.** Insufficient collaboration among academia, defence and industry hampers innovation and the transition of technology.

7.5. **Critical Material and Rare Earth Dependence.** Dependence on foreign sources for semiconductor materials and rare earth elements creates strategic vulnerabilities

7.6. **Inadequate Testing, Packaging and Validation Infrastructure.** Limited domestic capability for packaging, testing and validation slows technology deployment.

7.7. **Funding and Risk-Sharing Constraints.** High financial risk discourages private sector participation in defence semiconductor development.

7.8. **Limited Defence-Oriented Startup Ecosystem.** Emerging startups exist but require stronger policy support and defence integration.

CORE POLICY RECOMMENDATIONS

8. The core policy recommendations are as follows: -

8.1. **Doctrinal Employment Norms.**

8.1.1. **Integrate Semiconductors into Defence Doctrine.** Semiconductors should be treated as mission-critical operational enablers and incorporated into defence planning, capability development, and future force structuring.

8.1.2. **Standardisation of Indigenous Semiconductor Usage.** Common standards for security, interoperability, lifecycle management and technology refresh cycles should be defined to enable long-term sustainment.

8.1.3. **Lifecycle-Based Capability Planning.** Doctrinal norms should include lifecycle management, obsolescence handling and upgrade strategies for semiconductor-enabled defence systems.

8.2. **Need Identification.**

8.2.1. **Tri-Services Semiconductor Requirement Framework.** Establish a tri-services mechanism to identify and prioritise semiconductor needs across communications, sensors, AI, EW, and computing.

8.2.2. **Long-Term Demand Forecasting.** Develop a rolling 10-year semiconductor demand forecast aligned with future warfare and operational requirements.

8.2.3. **Translation of Operational Needs into Chip Specifications** Defence services, DRDO, and industry should jointly convert operational requirements into technical semiconductor specifications.

8.3. **Procurement Challenges.**

8.3.1. **Flexible Procurement Models.** Adopt developmental procurement, assured offtake, and phased acquisition to support indigenous semiconductor development.

8.3.2. **Incentivising Indigenous Development.** Procurement policies should prioritise indigenous semiconductor content and encourage participation from startups and MSMEs.

8.3.3. **Shift from L1 to Strategic Procurement.** Move beyond lowest-cost procurement to capability-based acquisition for strategic semiconductor technologies.

8.3.4. **Formation of a Joint Working Group of SHQ and HQ IDS.** A JWG is proposed to be formed to represent Armed Forces in the National Semiconductor Mission, which shall be including representations from SHQ and HQ IDS. Domain experts and Policy makers may be co-opted as members of this JWG.

8.4. **Trial and Testing Facilities.**

8.4.1. **Establish Dedicated Semiconductor Testing Facilities**. Create national-level facilities for radiation testing, environmental validation, and reliability assessment of defence-grade chips.

8.4.2. **Shared Test Infrastructure.** Enable DRDO, academia, startups, and industry access to a common testing and validation infrastructure.

8.4.3. **Accelerate Technology Maturity.** Robust testing facilities will reduce development timelines and improve deployment readiness of indigenous semiconductor solutions.

8.5. **Supply Chain (Semiconductor Ecosystem Resilience).**

8.5.1. **Develop End-to-End Indigenous Supply Chain.** Strengthen domestic capability in materials, fabrication, packaging, testing, and lifecycle support.

8.5.2. **Strategic Partnerships and Diversification.** Build trusted international partnerships and diversify sourcing to reduce dependency on single regions.

8.5.3. **Secure Supply Chain Frameworks.** Implement mechanisms for counterfeit detection, hardware security, and the sourcing of trusted components.

8.6. **Envisaged Support from Armed Forces / Users.**

8.6.1. **Armed Forces as Demand Drivers.** Defence services should specify operational requirements and serve as primary drivers of demand for indigenous semiconductor development.

8.6.2. **Support Joint Development and Trials.** Armed forces should participate in co-development programs and facilitate field trials in operational environments.

8.6.3. **Assured Procurement and Early Adoption.** Provide assured procurement and early induction of indigenous technologies to accelerate ecosystem growth.

9. **Need for the formation of a Joint Working Group (JWG).** A JWG is proposed to be formed to represent the Armed Forces in the National Semiconductor Mission, which shall include representations from the Tri-Services, HQ IDS, Domain experts and policymakers (MeitY). The JWG formed by the Lead Service can undertake the task and the outcome of the deliberations of JWG can become action points for MoD, MeitY, DRDO etc. This JWG will endeavour to reduce dependence on imports, promote domestic innovation, and support the development of next-generation technologies such as compound semiconductors, radiation-hardened chips, and secure processors. It will play a crucial role in enhancing India's defence preparedness, ensuring technological sovereignty and strengthening national security by fostering a resilient, indigenous semiconductor ecosystem.

10. **Initiative Recommendation for HQ IDS**.

10.1. A JWG consisting of representatives from SHQ and HQ IDS should be established under the chairmanship of SA to CISC to oversee all matters related to semiconductor planning, integration and policy for defence applications.

10.2. The JWG will discuss and put forward the demands of the Armed Forces to the technical working group of ISM under Meity. Experts from various compound semiconductor domains from academia/industry/R&D laboratories from various govt. depts. (including DRDO) will be co-opted on need basis.

10.3. JWG should define and formalize comprehensive operational requirements, clearly specifying the need for semiconductor components as an integral part of all equipment procurement across the three services.

10.4. The proposed JWG should translate these operational requirements into detailed technical specifications for semiconductor chips, ensuring their appropriate inclusion in procurement processes and system design.

10.5. In cases where chips meeting the exact required specifications are not available, the most suitable alternatives of indigenous origin should be selected to the extent feasible.

10.6. Where significant gaps exist between available semiconductor capabilities and operational requirements, appropriate doctrinal and tactical adjustments should be developed and implemented to mitigate capability shortfalls.

10.7. In scenarios involving critical capability gaps, the procurement of imported semiconductor chips may be considered, subject to stringent validation to ensure the absence of vulnerabilities such as backdoors, kill switches or unauthorized remote access mechanisms.

10.8. The requirement for secure, trusted semiconductor components—whether indigenous or imported without vulnerabilities—should be explicitly incorporated at the Request for Proposal (RFP) stage to ensure that operational security is not compromised during deployment or combat.

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11. **Critical Inputs for JWG.** With regards to the fab facilities in niche technologies (excluding Silicon CMOS), the strategic semiconductor policy framework should also consider following critical inputs:-

11.1. The private-sector fabs being set up are expected to operate on a return-on-investment (ROI) basis. The volume for defence-grade compound semiconductors is too low to sustain a private fab, leading to a market-driven failure that only the government can fill by prioritising national security over profit.

11.2. The specific recipes and architectures for military-grade chips are often classified. Private entities, especially those with international stakeholders, may face conflicts of interest or security leaks that a government-run facility can strictly prevent.

11.3. In a total war scenario, a government-controlled fab can be immediately pivoted to produce critical components without contractual negotiations or price gouging that might occur in the private sector.

11.4. These niche fab facilities can allow sharing of infrastructure with startups, academia, and industry partners and will become a hub for domestic IP generation following a whole-of-nation approach.

11.5. It may also be noted that both ISM 1.0 and 2.0 are more focused towards setting up fabs based on technology licensing from foreign technology IPs. To truly turn India into Viksit Bharat, we need to create domestic IPs not just in chip design but also in chip fabrication, particularly in compound semiconductors, photonics, quantum technology and MEMS. This can only be done by dedicated Research & Development. This requires strategic state-of-the-art facilities for the development of these niche technologies.

11.6. The existing defence centric fab facilities like GAETEC, Hyderabad and STARC, Bengaluru do not have adequate capacity to fulfil all the above requirements. In view of the above, these strategic facilities are required to be modernised with enhanced capacity to retain state control, ensuring that R&D remains aligned with the long-term roadmap of the Ministry of Defence. In addition, it is also necessary to set up a new facility to focus on niche emerging technologies like Quantum, THz and Photonics, which are going to be crucial for the next-generation battlefront.

11.7. It may be noted that MeitY is modernising the Silicon fab under its operational control, i.e. SCL, Mohali, through ISM 1.0 at a cost of ~4,500 Cr. Similar upgradation of GAETEC, Hyderabad is required to be carried out by MoD in its Strategic Semiconductor Policy push.

CONCLUSION

12. The 2nd workshop-cum-exhibition highlighted that semiconductor capability has emerged as a decisive enabler of modern warfare and a critical pillar of national security. The discussions underscored the urgent need for India to transition from dependence on foreign semiconductor ecosystems to a resilient, indigenous capability supported by a whole-of-nation approach. The evolving roles of defence forces as demand drivers, DRDO as a technology integrator, and industry and academia as innovation partners reflect a significant shift toward a collaborative national innovation model. The emphasis on doctrinal integration, structured need identification, flexible procurement, robust testing infrastructure, and resilient supply chains collectively points toward building a secure and self-reliant semiconductor ecosystem aligned with future warfare requirements.

13. The workshop further emphasized that achieving semiconductor sovereignty requires mission-mode execution, long-term policy stability, and coordinated stakeholder engagement. Envisaged support from DRDO and armed forces, along with strengthened industry participation and indigenous IP development, will be critical to accelerating innovation and reducing technological gaps. By leveraging India's strong design talent, fostering trusted global partnerships, and building end-to-end domestic capabilities, India can build a sustainable, export-oriented semiconductor ecosystem. Timely implementation of these policy recommendations will enhance operational readiness, strengthen technological sovereignty, and position India as a key global player in defence semiconductor technologies.