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WEB ARTICLE
WA/13/26

**SILICON SOVEREIGNTY:
SEMICONDUCTORS &
STRATEGIC COMPUTE FOR
BATTLEFIELD AI
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Strengthening India's AI Defence Chip Ecosystem: RISC-V for UAVs, Secure Processors for Tactical Edge Computing, Indigenous Design for Next-Generation Battlefield AI

Wars of tomorrow will not be won only by the soldier who pulls the trigger; they will be decided by the algorithm that processes the intelligence a millisecond faster. For India, that algorithm needs to run on an Indian chip.

The Compute Imperative

Across the flash-points of the twenty-first century, from the drone-saturated skies over Ukraine to the high-altitude standoffs along India's northern borders, a quiet but decisive technological contest is playing out beneath the kinetic one. Nations that can design, manufacture, and deploy advanced semiconductors at the tactical edge of warfare will hold an asymmetric strategic advantage. For India, a country that imports over a billion chips a year while simultaneously aspiring to become a next-generation military power, the calculus is both urgent and unambiguous: indigenous

semiconductor capability is no longer merely an economic aspiration; it is a national security imperative.¹

Indian Defence Minister Rajnath Singh captured the shift with stark clarity in October 2025: *"The battlefield has changed. Wars of tomorrow will be fought with algorithms, autonomous systems and artificial intelligence. Drones, anti-drone systems, quantum computing and directed-energy weapons will define the future."*² These are not rhetorical flourishes. India now has more than 300 defence-focused AI projects underway across DRDO, the armed services, defence public sector undertakings, and iDEX startups.³

Every single one of those projects, every autonomous drone, every AI-fused surveillance feed, every real-time C4ISR dashboard, depends on a semiconductor at its computational core. Yet the chips powering India's battlefield AI today are overwhelmingly foreign-made. That dependence exposes military-grade systems to supply-chain disruption, potential hardware backdoors, export-control leverage by adversaries, and the kind of catastrophic technological denial that a full-spectrum conflict could easily trigger. Closing this gap, through a deliberate, architecturally sound, and institutionally backed indigenous chip ecosystem, is the strategic challenge this article examines.

300+ Defence-focused AI projects in India (2025)	₹6.81L Cr India's Defence Budget FY 2025-26
1 Billion+ Chips imported annually by India	\$11 Billion Tata semiconductor fab investment, Dholera
460% Rise in Indian chip startup funding (2023-24)	30.7% Global RISC-V market CAGR (2025-2034)

Table 1: Source: Author's compilation from various sources

RISC-V: The Architecture of Strategic Anatomy

At the heart of India's indigenous chip push lies an architectural decision with profound strategic consequences: the adoption of RISC-V (Reduced Instruction Set Computing, Fifth Generation) as the foundational Instruction Set Architecture (ISA)

for defence-grade processors. Unlike the proprietary architectures offered by Intel/AMD (x86) and ARM, both of which require expensive licensing and, crucially, are subject to foreign export controls, RISC-V is an open standard managed by the non-profit RISC-V International. ⁴

This openness carries military-grade significance. A nation building its battlefield AI on ARM or x86 processors is, in a very real sense, running its national security infrastructure on intellectual property owned by a foreign entity. RISC-V eliminates that dependency, enabling India's chip designers to implement, customise, and harden the architecture without licensing fees, foreign IP exposure, or the risk of technology denial.⁵ The global RISC-V market was valued at USD 1.76 billion in 2024 and is forecast to grow at a compound annual rate of 30.7 per cent through 2034, reaching over USD 25 billion.⁶

India's semiconductor ecosystem has recognised this early. IIT Madras's landmark SHAKTI project, developed in collaboration with ISRO, produces open-source, industrial-grade RISC-V processors. ISRO itself unveiled the Vikram-32 processor at SEMICON India 2025, a highly energy-efficient, RISC-V-based microprocessor designed for embedded and space-grade applications.^{7,8}

On the commercial side, IIT Madras spin-off InCore Semiconductors has developed the 'Vrinda AI' chip for on-device machine learning, while Mindgrove Technologies has launched India's first indigenously designed commercial high-performance MCU chip and is now working on a Vision SoC explicitly designed for edge AI applications. These chips are priced approximately 30 per cent below equivalent international competitors.⁹ Most strikingly, Bengaluru-based CalligoTech has introduced TUNGA, described as the world's first Posit-enabled RISC-V CPU for AI and high-performance computing. ¹⁰

KEY RISC-V ADVANTAGES FOR DEFENCE APPLICATIONS
▶ No foreign IP exposure , eliminates risk of technology denial in conflict scenarios
▶ Full customisability , hardware security extensions, side-channel mitigations, domain-specific acceleration added at the ISA level
▶ Cost-efficient , no per-unit royalties; ~30% cheaper than ARM-based solutions at the systems level

<ul style="list-style-type: none"> ▸ Open-source toolchains , enables secure, fully auditable software stacks (Linux, FreeRTOS, Zephyr)
<ul style="list-style-type: none"> ▸ Scalable across SWaP domains , from IoT sensors to edge AI accelerators to mission computers
<ul style="list-style-type: none"> ▸ Precedent in critical applications , NASA JPL spaceflight computing; DARPA hardware architecture security

Table 2: Source: Author’s compilation from various sources

Tactical Edge Computing: The New Battlefield Nervous System

The modern battlefield is a data ecosystem. Satellites, drones, EO/IR cameras, seismic sensors, synthetic aperture radars, and electronic intelligence collectors pour torrents of information into military networks. The decisive question is no longer whether to collect that data, but whether to process it at the source (the edge) or transmit it to a remote data centre for analysis. The answer, for battlefield AI, is unambiguous: compute at the edge, where latency is measured in milliseconds and where connectivity to rear-area servers cannot be guaranteed.

India's Indian Army has already deployed over 140 AI-based surveillance platforms across the Line of Control (LoC) and Line of Actual Control (LAC), integrating multi-sensor inputs including EO/IR cameras, UAV feeds, and SAR data.¹¹ These systems depend on processors embedded in rugged field units that can perform computer vision inference, target classification, and anomaly detection without cloud connectivity. This is the domain of the *tactical edge processor*, demanding chips that are simultaneously powerful enough to run neural network inference, hardened against physical tampering and electromagnetic attacks, and sufficiently power-efficient for deployment on unmanned platforms.

Current Indian solutions in this space are nascent but promising. Tonbo Imaging supplies thermal-imaging modules embedded with CNN-based object classifiers for sniper scopes and UAV payloads.¹² Netrasemi raised USD 13 million in 2024 to build a dedicated semiconductor manufacturing facility for Edge AI chips.¹³ Morphing Machines in Bengaluru is exploring neuromorphic AI accelerators based on reconfigurable architectures for low-power applications, a critical capability for long-endurance UAVs, where power efficiency directly translates to mission range.¹⁴

The key architectural challenge for tactical edge compute is the security layer. Foreign-designed processors may contain undisclosed hardware backdoors, a risk that is not theoretical. For mission-critical applications, encrypted C2 links, target discrimination algorithms, and IFF (Identification Friend or Foe) processing, the processor itself must be trustworthy at the hardware level. This requires the design of secure enclaves, hardware root-of-trust implementations, and physically unclonable functions (PUFs) from the ground up. That level of hardware assurance is only achievable through indigenous chip design.

"We must not remain imitators or followers in technology; we must become the creators and standard-setters for the world."

-Raksha Mantri Rajnath Singh, iDEX National Conference, October 2025

RISC-V for UAVs: From Swarms to Loitering Munitions

The unmanned aerial vehicle has become the defining weapons system of contemporary warfare. India's own battlefield experience and the lessons drawn from conflicts in the Caucasus, the Levant, and Eastern Europe have accelerated UAV integration across all three services. The Indian Army is already fielding AI-enabled drones for reconnaissance along disputed borders, while iDEX has funded the development of swarming drones, loitering munitions, and beyond-visual-line-of-sight (BVLOS) logistics platforms.¹⁵

The computational demands of an autonomous tactical UAV are severe. A reconnaissance drone must run real-time computer vision for target detection; a loitering munition must execute on-board terminal guidance with GPS-denied navigation fallback; a swarm member must participate in distributed coordination protocols with minimal latency. All of this must happen within a Size, Weight, and Power (SWaP) envelope that is acutely constrained by aerodynamic and endurance requirements.

RISC-V-based System-on-Chips (SoCs) are uniquely positioned to address this challenge. The architecture's modularity allows designers to integrate only the processor cores, hardware accelerators, and peripherals needed for a specific UAV mission profile. A RISC-V UAV mission computer might integrate a multi-core RISC-V CPU cluster alongside a custom neural network accelerator tensor core, a

hardware-accelerated flight controller interface, a cryptographic engine for secure communications, and an anti-tamper module, all on a single die, designed and certified in India.

DRDO's Centre for Artificial Intelligence and Robotics (CAIR) has developed over 75 AI-based defence products, including autonomous platforms and AI surveillance systems.¹⁶ DRDO's Netra UAV already integrates AI algorithms for automated object recognition and target classification.¹⁷ The next step, one that the India Semiconductor Mission must explicitly prioritise, is to replace the foreign-origin processors powering these systems with domestically designed RISC-V SoCs.

India's drone sector received additional impetus from Operation Sindoor (May 2025), which demonstrated in an operational setting the criticality of indigenous drone and counter-drone capabilities. Several iDEX startups were commended by the defence minister for their role in the operation, signalling that the pipeline from lab to battlefield is shortening.¹⁸

The Policy Architecture: ISM, iDEX, DLI, and the Missing Link

India's semiconductor and defence innovation ecosystem has been built on a sequence of progressive policy interventions. The India Semiconductor Mission (ISM), launched in 2021 with an initial commitment of approximately USD 10 billion, established the foundational investment framework for chip and display fabrication.¹⁹ The Design Linked Incentive (DLI) Scheme (2022) has been the more operationally consequential instrument for the defence chip pipeline: by mid-2025, New Delhi had approved 23 chip design projects and provided 72 companies access to high-quality Electronic Design Automation (EDA) tools.²⁰

On the defence innovation side, iDEX has supported over 300 startups and MSMEs, with ADITI funding projects at higher Technology Readiness Levels with grants up to Rs. 25 crore.²¹ The Defence Artificial Intelligence Council (DAIC), chaired by the Raksha Mantri, provides strategic oversight on cross-service AI adoption.²²

Despite these advances, a structural gap persists: *the absence of a dedicated programme linking semiconductor design to defence qualification and procurement.* A chip developed under the DLI scheme exists in a civilian innovation pathway. To cross into defence use, it must clear MIL-SPEC qualification processes that can take

years. India needs a Defence Semiconductor Integration Programme (DSIP), a joint MeitY-MoD initiative, to create a fast-track qualification framework for RISC-V processors, fund ruggedisation testing of indigenous chip designs, provide assured procurement commitments for defence-grade semiconductor components, and establish a classified fabless design centre under DRDO with a direct pipeline to Tata's Dholera fab. ²³

ECOSYSTEM ACTORS, INDIA'S DEFENCE CHIP PIPELINE
▶ IIT Madras / SHAKTI Project, RISC-V processor cores, aerospace-grade; partnered with ISRO
▶ Mindgrove Technologies, Secure IoT MCU; Vision SoC for edge AI surveillance
▶ InCore Semiconductors, 'Vrinda AI' chip for on-device ML; optimized RISC-V
▶ CalligoTech (TUNGA), World's first Posit-enabled RISC-V CPU for AI / HPC
▶ Morphing Machines (REDEFINE), Neuromorphic AI accelerator; reconfigurable many-core
▶ AGNIT Semiconductors, GaN-based power semiconductors for defence / telecom
▶ Saankhya Labs, SDR chipsets (Pruthvi series); 5G and satellite comms SoCs
▶ Netrasemi, Edge-AI chip; USD 13M manufacturing facility (2024)
▶ Tata Electronics (Dholera fab), USD 11B mega-fab; production projected ~2027

Table 3: Source: Author's compilation from various sources

Secure Processors: The Hardware Trust Problem

The most challenging and technically complicated task of a defence chip is hardware security. The AI system depends on silicon for power and reliability. The level of threat posed by state-level attackers is not considered during the design of commercial processors. The processors are designed to serve globally at a large scale. They might have a secret debug interface, micro architectural flaws, and a management framework. A skilled enemy can take advantage of that weakness. Spectre and Meltdown are well-known examples.

Three threat layers are introduced to secure access to the processor utilised for next-generation battlefield AI in India. At the hardware level, a processor incorporates hardware as a root of trust. The secure boot ROM, HSM, and PUFs bind cryptographic identity. At the architectural layer, secure enclaves isolate and classify inference workload from the general operation scale. At the supply chain level, chips need to be designed so they cannot be hacked. Chips also need to be manufactured in a domestic facility. Also undetectable after the formulation through X-ray tomography.

The initiative taken by DRDO through its QTRC (Quantum Technologies Research Centre) was established in 2025. It is developing a quantum secure communication distribution technique. That technique covers more than 1 kilometre of surveillance area.²⁴ Hardware-level secure processor program, translating quantum-resistant cryptographic algorithms into silicon implementations on RISC-V platforms to perform the efforts.

Recommendations: A Roadmap for Indigenous Battlefield AI Chips

Establish a Defence RISC-V Processor Programme (DRPP): MoD and MeitY should jointly establish a classified programme to develop a family of RISC-V processors specifically qualified for defence use: a low-power UAV mission computer SoC, a tactical edge inference accelerator, and a secure communications processor. The SHAKTI and InCore architectures provide the natural starting point.

- **Fast-Track Tata Dholera for Military Process Nodes**

The Dholera fab should be prioritised for a dedicated military process allocation, similar to how TSMC's US Arizona fabs have been structured for US DoD 'trusted foundry' access. A classified government-to-company agreement establishing a secure production line for defence chips with independent supply-chain verification would close the fabrication gap within the decade.

- **Create the Defence Semiconductor Integration Programme (DSIP)**

A formal bridge programme between the DLI scheme and defence qualification pathways would transform India's growing chip design community into a genuine contributor to the defence industrial base. Assured procurement commitments must explicitly include semiconductor components, not just systems-level platforms.

- **Invest in Edge AI Silicon for UAV Swarms**

A dedicated solicitation under ADITI/iDEX for indigenous RISC-V-based UAV mission computers, with defined performance, SWaP, and security requirements, would create a demand signal sufficient to pull private-sector investment into mil-grade chip design.

- **Build the Engineering Pipeline**

Investor funding in Indian chip startups surged 460 per cent from USD 5 million in 2023 to over USD 28 million in 2024.²⁵ Capital alone will not sustain an ecosystem: talent will. SEMI's Indian Semiconductor Academy, combined with expanded EDA tool access under DLI and a structured DRDO-industry-academia partnerships modelled on the IIT Madras Robert Bosch Centre collaboration, must generate the next generation of chip architects who understand both silicon and strategy.

Conclusion: Silicon is the New Steel

It is clear from the US-China semiconductor war of 2021 that chip shortages are crucial. The semiconductor supply chain is now a strategic scenario for national power. India is becoming a nation with good engineering talent. Government commitment and security parameters are important, but the question is the semiconductor ecosystem. In a quickly growing technological world, the country has more steel and a strong ecosystem.

The RISC-V version of the architecture is available. IIT Madras and the expanding startup sector, which includes companies like Mindgrove and CalligoTech, are home to talented designers. At Dholera, the manufacturing infrastructure is being built. 300 defence AI projects and a defence budget of Rs. 6.81 lakh crore represent the demand signal. What remains is the institutional will to connect these pieces, to build the bridge between chip design lab and battlefield deployment, before the next conflict makes the cost of inaction catastrophic. Silicon sovereignty is not a luxury. It is the foundation upon which every other element of India's battlefield AI ambition rests.

DISCLAIMER

The paper is the author's individual scholastic articulation and does not necessarily reflect the views of CENJOWS, the Defence forces or the Government of India. The author certifies that the article is original in content, unpublished, and it has not been submitted for publication/ web upload elsewhere and that the facts and figures quoted are duly referenced, as needed and are believed to be correct.

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